Product Summary

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
30V	6.5mΩ@10V	12A
	8mΩ@4.5V	

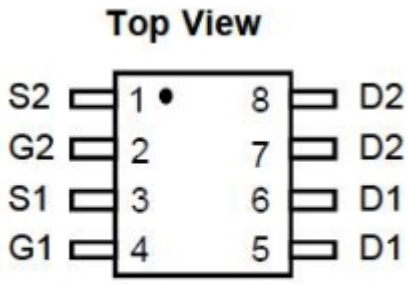
Feature

- V_{DS} =30V,I_D =12A
- $R_{DS(ON)}$ < 8mΩ @ V_{GS}=10V
  $R_{DS(ON)}$) <13mΩ @ V_{GS}=4.5V
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current

Application

- Power switching application
- Uninterruptible Power Supply

Package



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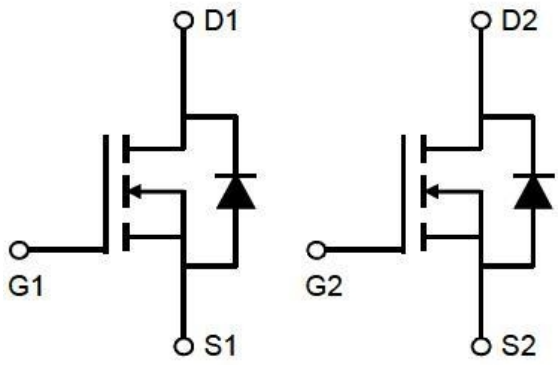
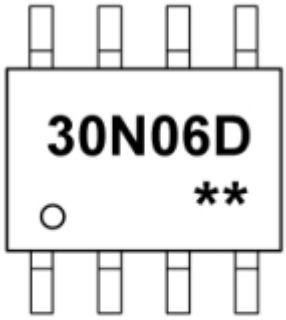
Circuit diagram



Marking



30N06D =Device Code
** =Week Code

Absolute maximum ratings

(T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	12	A
Pulsed Drain Current	I_{DM}	48	A
Maximum Power Dissipation	P_D	2.5	W
Single pulse avalanche energy [1]	E_{AS}	57.8	mJ
Thermal Resistance,Junction-to-Case[2]	$R_{\theta JC}$	50	℃/W
Operating Junction and Storage Temperature Range	T_{STG}, T_J	-55 To 175	℃

Electrical characteristics

(T_A=25℃, unless otherwise noted)

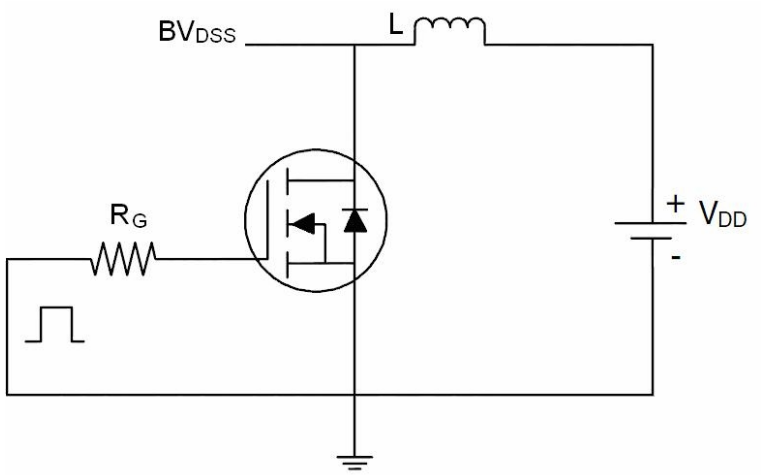
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	$BV_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	30			V
Zero gate voltage drain current	I_{DSS}	V_{DS} =30V, V_{GS} = 0V			1	uA
Gate-body leakage current	I_{GSS}	V_{DS} =0V,V_{GS} =±20V			±100	uA
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1	1.5	2.5	V
Drain-source on-resistance	$R_{DS(on)}$	V_{GS} =10V, I_D =10A		6.5	8	mΩ
		V_{GS} =4.5V, I_D =5A		8	13	
Forward Transconductance	g_{FS}	V_{DS} =5V, I_D =10A	15			
Dynamic Characteristics[4]						
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=1MHz		1550		pF
Output Capacitance	C_{oss}			300		
Reverse Transfer Capacitance	C_{rss}			180		
Switching Characteristics[4]						
Turn-on Delay Time	$T_{d(on)}$	V_{DD}=25V, V_{GS}=10V, I_D =10A, R_{GEN}=6Ω		30		nS
Turn-on Rise Time	T_r			20		
Turn-off Delay Time	$T_{d(off)}$			100		
Turn-off Fall Time	T_f			80		
Total Gate Charge	Q_g	V_{DS}=15V, I_D =10A, V_{GS}=5V		13		pF
Gate-Source Charge	Q_{gs}			5.5		
Gate-Drain(“Miller”) Charge	Q_{gd}			3.5		
Drain-Source Diode Characteristics						
Diode Forward Voltage[3]	V_{SD}	V_{GS}=0V, I_S=1A			1.2	V

Notes:

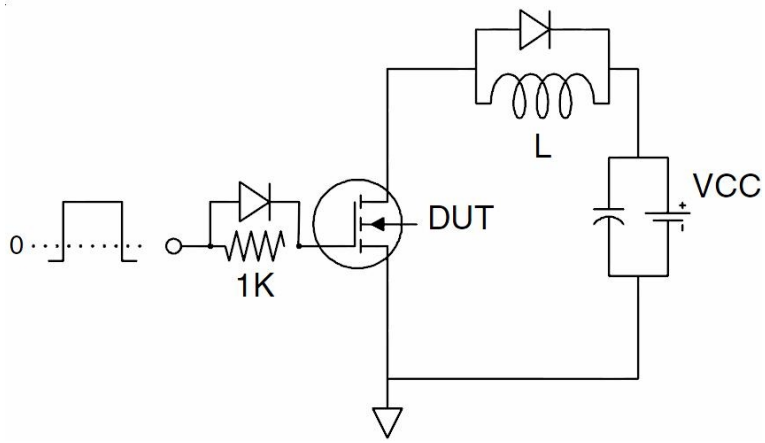
1. E_{AS} condition :Tj=25 ℃,V_{DD}=25V,V_G=10V,L=0.1mH
2. Repetitive Rating: Pulse width limited by maximum junction temperature.
3. Surface Mounted on FR4 Board, t ≤ 10 sec.
4. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
5. Guaranteed by design, not subject to production

Test Circuit

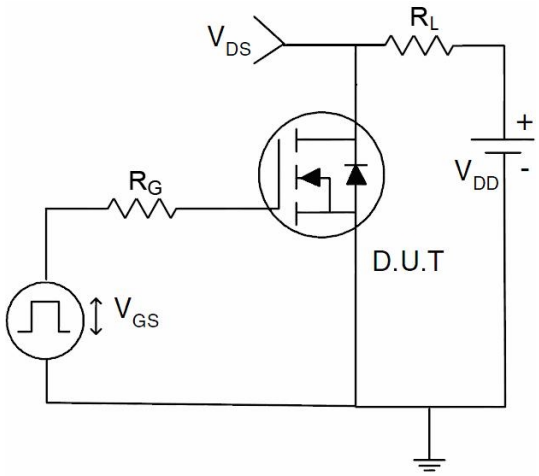
- EAS Test Circuits



- Gate Charge Test Circuit



- Switch Time Test Circuit



Typical Characteristics

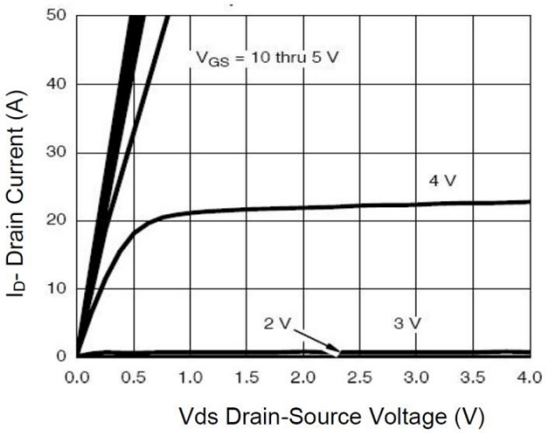


Figure 1 Output Characteristics

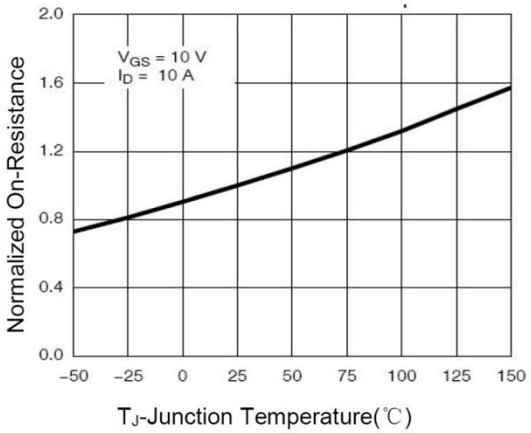


Figure 4 Rdson-JunctionTemperature

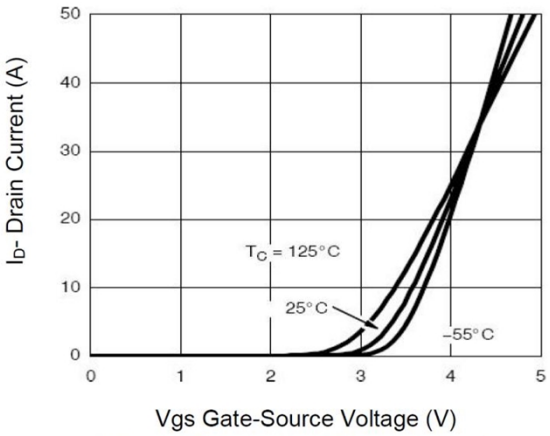


Figure 2 Transfer Characteristics

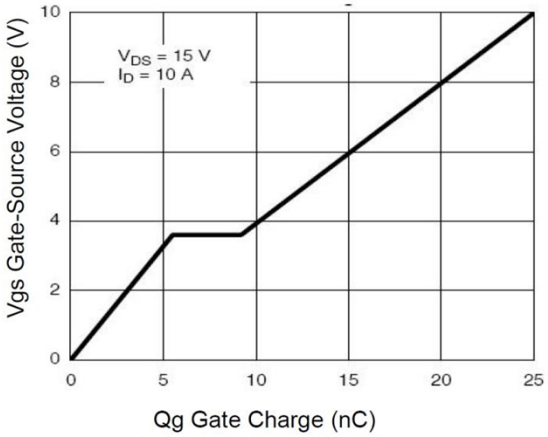


Figure 5 Gate Charge

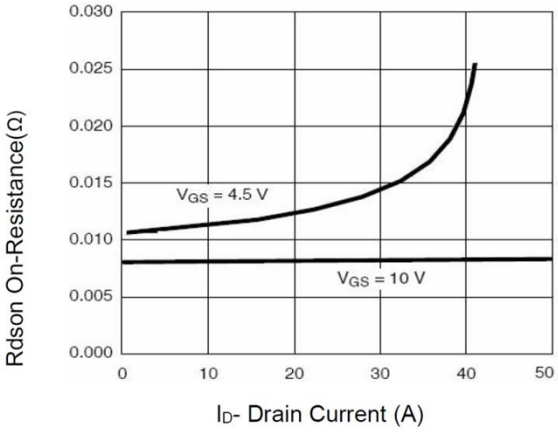


Figure 3 Rdson- Drain Current

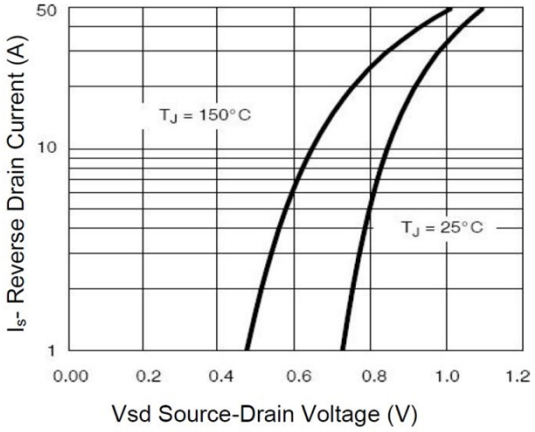


Figure 6 Source- Drain Diode Forward

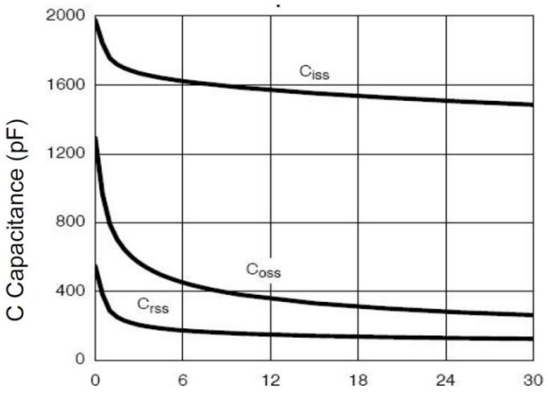


Figure 7 Capacitance vs Vds

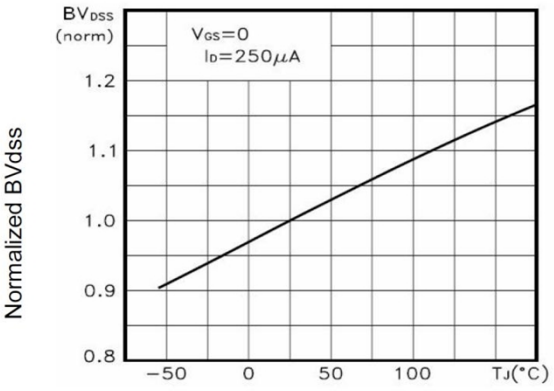


Figure 9 BV_{DSS} vs Junction Temperature

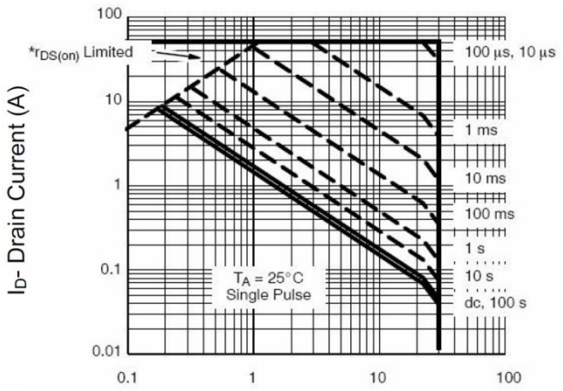


Figure 8 Safe Operation Area

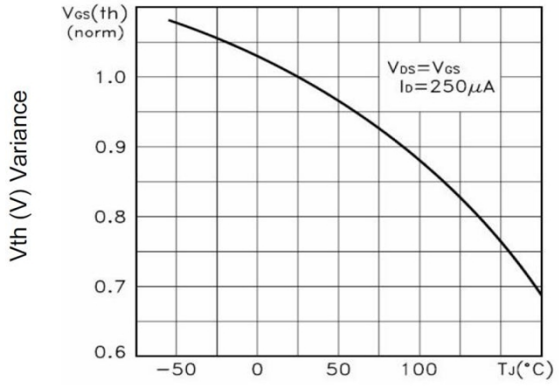


Figure 10 $V_{GS(th)}$ vs Junction Temperature

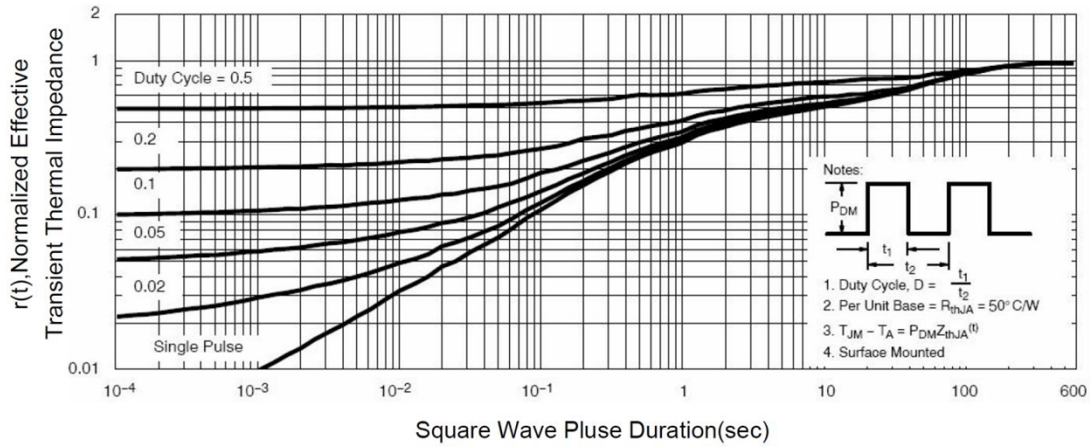
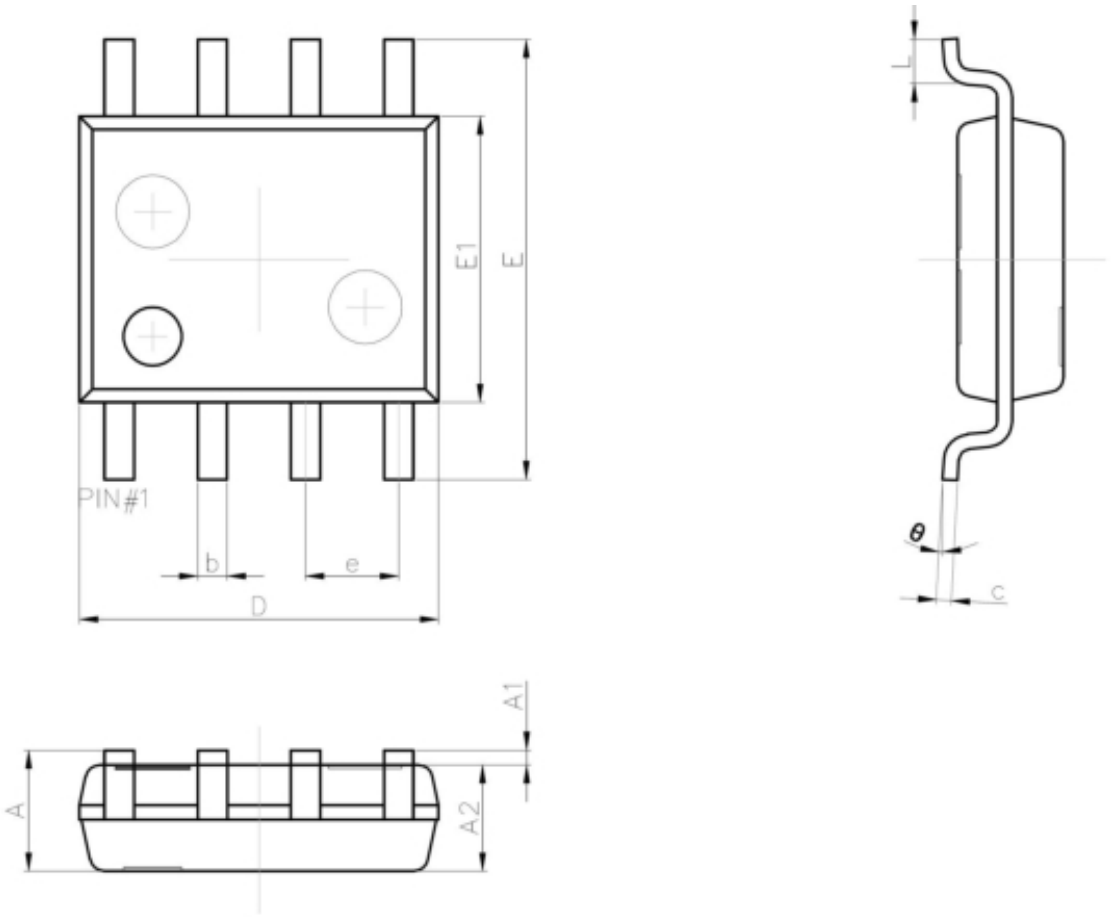


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information



Symbol	Dimensions In Millimeters	
	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
A2	1.35	1.55
b	0.33	0.51
c	0.17	0.25
D	4.80	5.00
e	1.27 REF.	
E	5.80	6.20
E1	3.80	4.00
L	0.40	1.27
θ	0°	8°