

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	I_D
100V	90mΩ@10V	10A

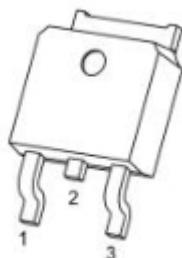
Feature

- $V_{DS} = 100V, I_D = 10A$
- $R_{DS(ON)} < 110m\Omega$ @ $V_{GS}=10V$ (Typ:90mΩ)
 $R_{DS(ON)} < 120m\Omega$ @ $V_{GS}=4.5V$ (Typ:100mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

Application

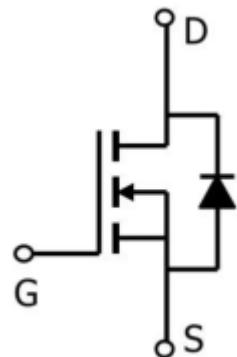
- Power switching application
- Load switching
- Uninterruptible power supply

Package

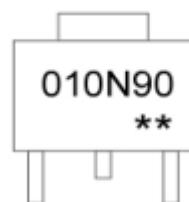


TO-252(G:1 D:2 S:3)

Circuit diagram



Marking



010N90 : Product code
 ** : Week code.

Absolute maximum ratings

($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	10	W
Pulsed Drain Current	I_{DM}	40	A
Maximum Power Dissipation	P_D	34	W
Thermal Resistance Junction-to-Case ¹	$R_{\theta JC}$	4.4	$^\circ\text{C}/\text{W}$
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +175	$^\circ\text{C}$

Electrical characteristics

($T_A=25^\circ\text{C}$, unless otherwise noted)

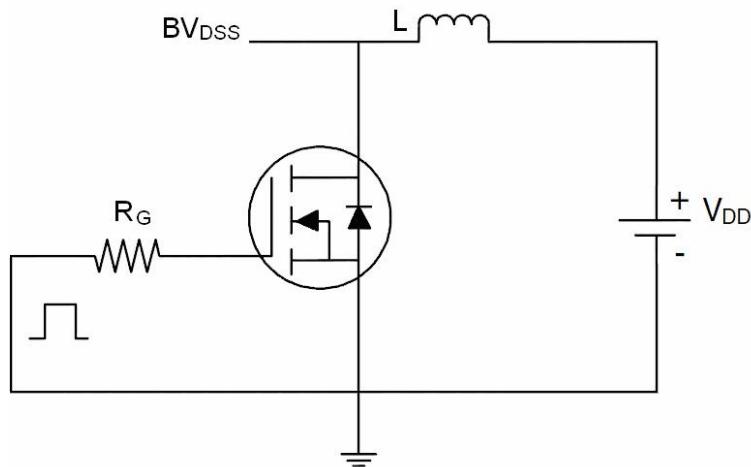
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static Characteristics						
Drain-source breakdown voltage	BV_{DSS}	$V_{\text{GS}} = 0\text{V}, I_{\text{D}} = 250\mu\text{A}$	100			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 100\text{V}, V_{\text{GS}} = 0\text{V}$			1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{\text{GS}} = \pm 20\text{V}, V_{\text{DS}} = 0\text{V}$			± 100	μA
Gate threshold voltage	$V_{\text{GS(th)}}$	$V_{\text{DS}} = V_{\text{GS}}, I_{\text{D}} = 250\mu\text{A}$	1.0	1.6	2.5	V
Drain-Source On-State Resistance	$R_{\text{DS(on)}}$	$V_{\text{GS}} = 10\text{V}, I_{\text{D}} = 10\text{A}$		90	110	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_{\text{D}} = 8\text{A}$		100	120	
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 25\text{V}, I_{\text{D}} = 6\text{A}$	3.5			S
Dynamic characteristics⁴						
Input Capacitance	C_{iss}	$V_{\text{DS}} = 50\text{V}, V_{\text{GS}} = 0\text{V}, f = 1\text{MHz}$		800		pF
Output Capacitance	C_{oss}			39		
Reverse Transfer Capacitance	C_{rss}			32		
Switching Characteristics⁴						
Turn-On Delay Time	$T_{\text{d(on)}}$	$V_{\text{DD}} = 50\text{V}, R_{\text{L}} = 6.4\Omega, V_{\text{GS}} = 10\text{V}, R_{\text{GEN}} = 3\Omega$		5		nS
Rise Time	T_{r}			40		
Turn-Off Delay Time	$T_{\text{d(off)}}$			20		
Fall Time	T_{f}			7		
Total Gate Charge	Q_{g}	$V_{\text{DS}} = 50\text{V}, I_{\text{D}} = 10\text{A}, V_{\text{GS}} = 10\text{V}$		16		nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			2.6		
Drain-Source Diode Characteristics						
Diode forward voltage ³	V_{SD}	$V_{\text{GS}} = 0\text{V}, I_{\text{s}} = 15\text{A}$			1.2	V
Diode Forward Current ²	I_{s}				15	A
Reverse Recovery Time	t_{rr}	$T_j = 25^\circ\text{C}, I_F = 10\text{A}$ $dI/dt = 100\text{A}/\mu\text{s}(\text{Note3})$		21		nS
Reverse Recovery Charge	Q_{rr}			97		
Forward Turn-On Time	t_{ON}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

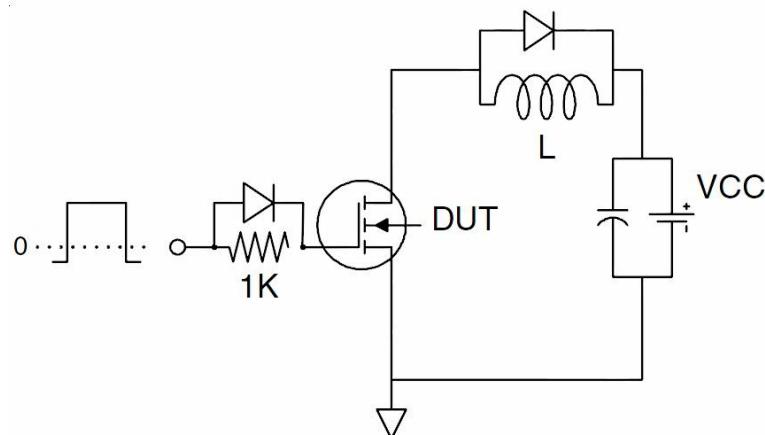
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.
3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production
5. EAS condition: $T_j = 25^\circ\text{C}, V_{\text{DD}} = 50\text{V}, V_{\text{G}} = 10\text{V}, L = 0.5\text{mH}, R_g = 25\Omega$

Test Circuit

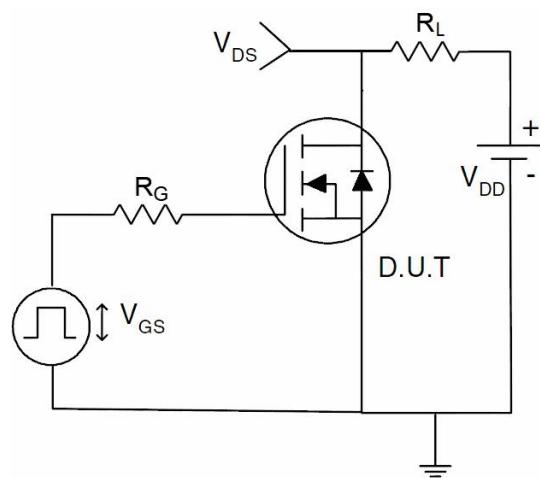
- EAS Test Circuits



- Gate Charge Test Circuit



- Switch Time Test Circuit



Typical Characteristics

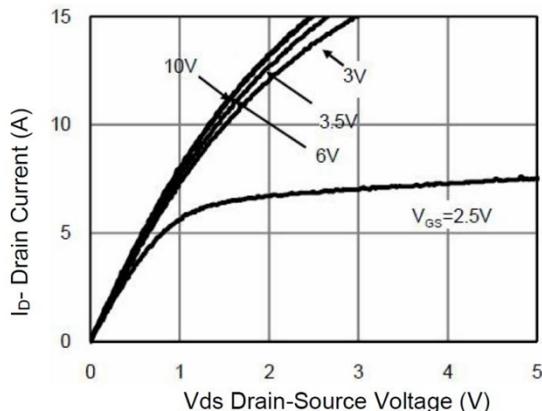


Figure 1 Output Characteristics

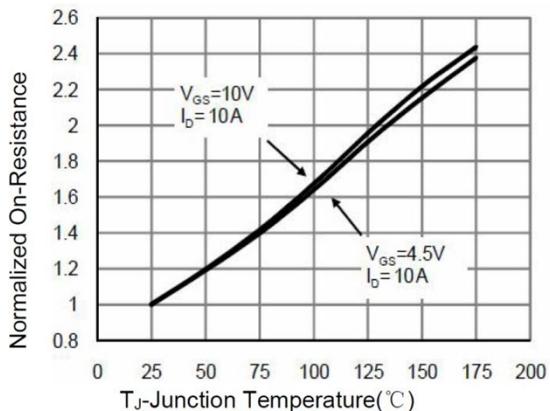


Figure 4 $R_{DS(on)}$ -JunctionTemperature

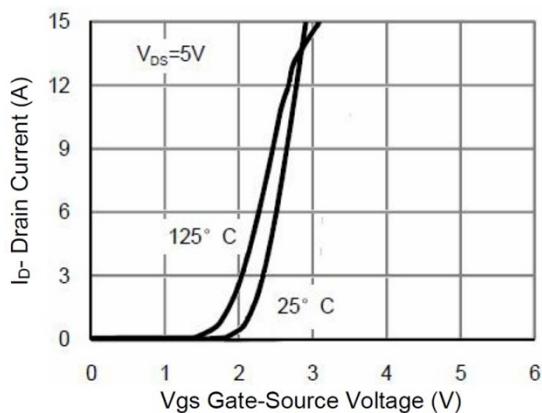


Figure 2 Transfer Characteristics

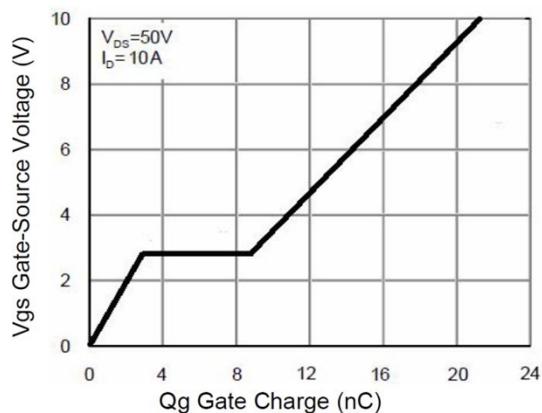


Figure 5 Gate Charge

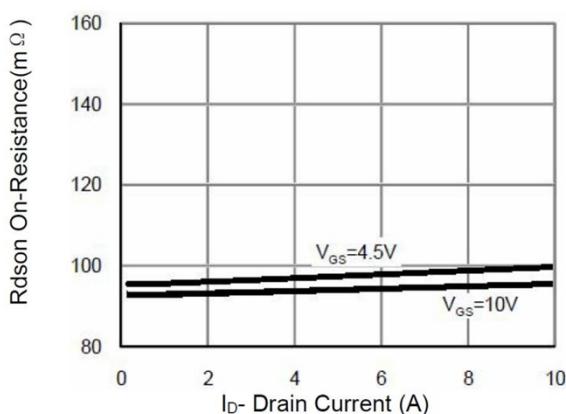


Figure 3 $R_{DS(on)}$ - Drain Current

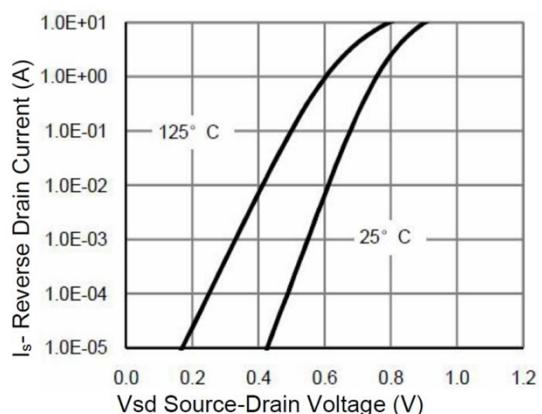
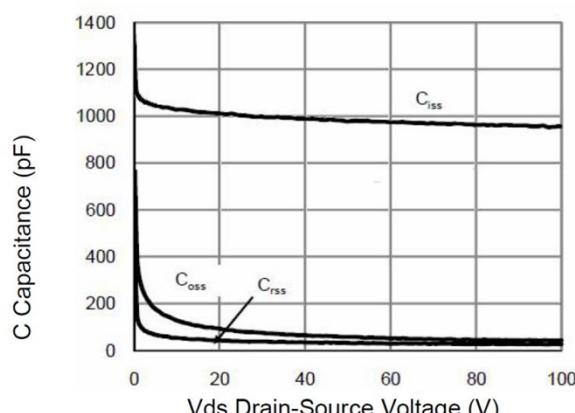
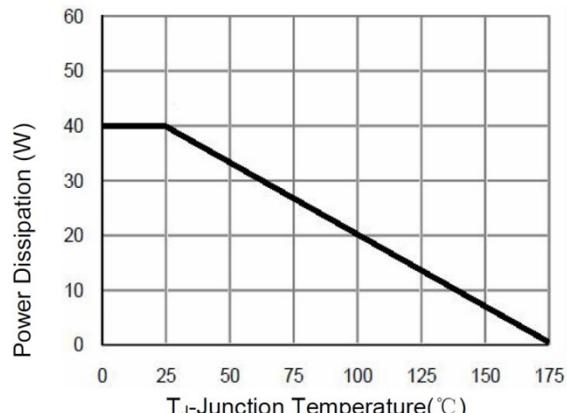
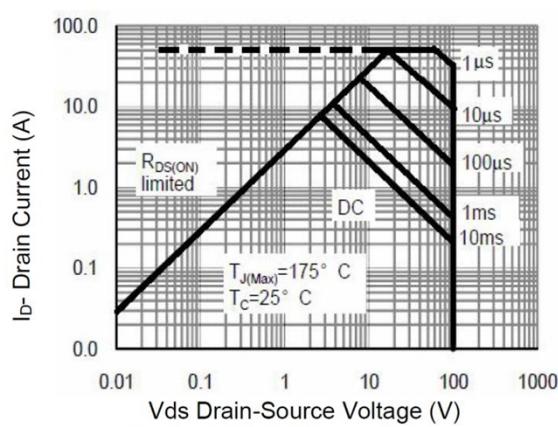
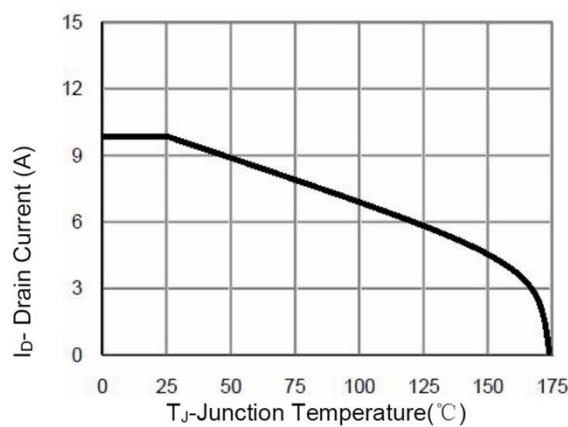
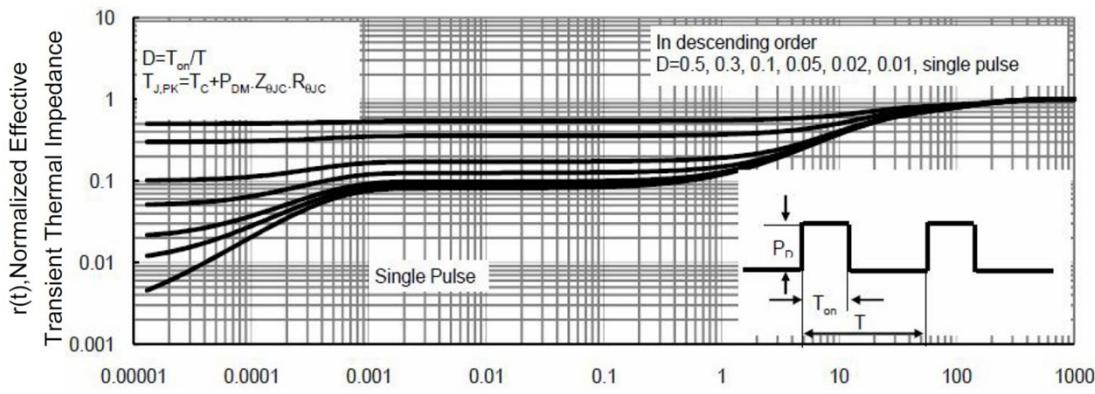
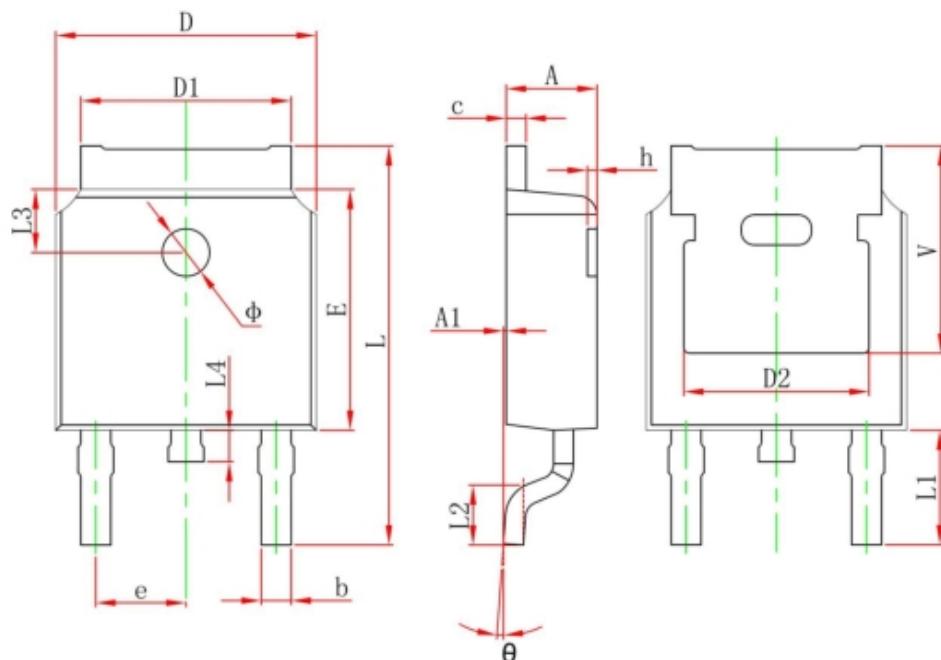


Figure 6 Source- Drain Diode Forward


Figure 7 Capacitance vs Vds

Figure 9 Power De-rating

Figure 8 Safe Operation Area

Figure 10 Current De-rating

Figure 11 Normalized Maximum Transient Thermal Impedance

TO-252 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 REF.		0.190 REF.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 REF.		0.114 REF.	
L2	1.400	1.700	0.055	0.067
L3	1.600 REF.		0.063 REF.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 REF.		0.211 REF.	