

## Product Summary

$V_{(BR)DSS}$	$R_{DS(on)TYP}$	$I_D$
40V	8mΩ@10V	50A
	11mΩ@4.5V	

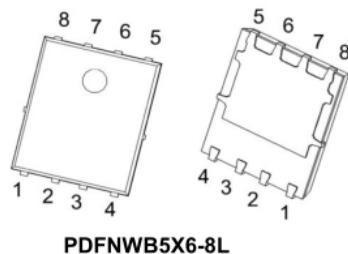
## Feature

- $V_{DS} = 40V, I_D = 50A$
- $R_{DS(ON)} < 11m\Omega$  @  $V_{GS} = 10V$  (Typ. 8 mΩ)
- $R_{DS(ON)} < 17m\Omega$  @  $V_{GS} = 4.5V$  (Typ. 11 mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current

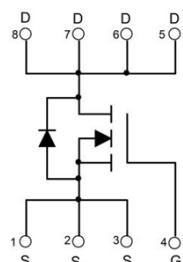
## Application

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

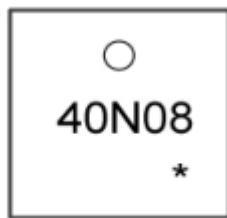
## Package



## Circuit diagram



## Marking



40N08 : Product code  
 \* : Month code.

## Absolute maximum ratings

( $T_a=25^\circ\text{C}$  unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		$V_{DS}$	40	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>(Note 4)</sup>	$T_C=25^\circ\text{C}$	$I_D$	50	A
Pulsed Drain Current <sup>(Note 1)</sup>	$T_C=25^\circ\text{C}$	$I_{DM}$	200	A
Power Dissipation	$T_C=25^\circ\text{C}$	$P_D$	83.8	W
	$T_C=100^\circ\text{C}$		41.9	
Continuous Drain Current <sup>(Note 4)</sup>	$T_C=25^\circ\text{C}$	$I_D$	11	A
	$T_C=70^\circ\text{C}$		9	
Power Dissipation	$T_C=25^\circ\text{C}$	$P_D$	2.4	W
	$T_C=70^\circ\text{C}$		1.6	
Single Pulse Avalanche Energy (Note 6)		$E_{AS}$	72	mJ
Typical Thermal Resistance (Note 4,5)	Junction to Case	$R_{\theta JC}$	1.79	°C/W
	Junction to Ambient	$R_{\theta JA}$	62.5	
Operating Junction and Storage Temperature Range		$T_J, T_{STG}$	-55 to 175	°C

## Electrical characteristics

( $T_A=25^\circ\text{C}$ , unless otherwise noted)

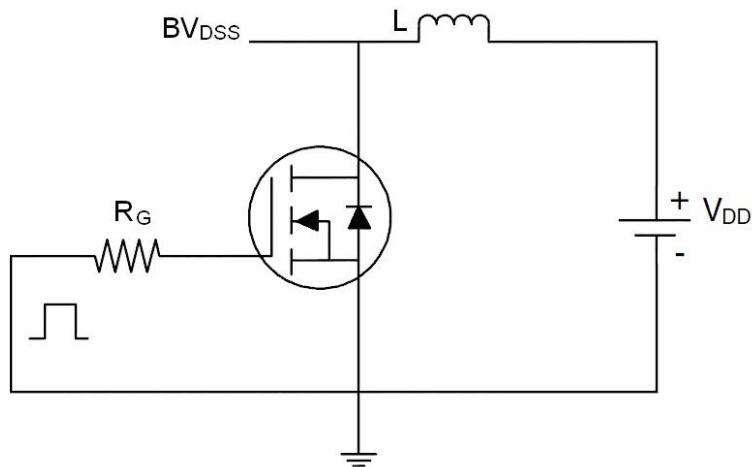
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$\text{BV}_{(\text{BR})\text{DSS}}$	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	40			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1	1.5	2.5	V
Drain-Source On-State Resistance	$R_{DS(\text{on})}$	$V_{GS} = 10\text{V}, I_D = 12\text{A}$		8	12	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 6\text{A}$		11	18	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$			1	$\mu\text{A}$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			100	$\mu\text{A}$
<b>Dynamic Characteristics<sup>(3)</sup></b>						
Total Gate Charge	$Q_g$	$V_{DS} = 20\text{V}, I_D = 8\text{A}, V_{GS} = 10\text{V}$ (Note 2,3)		22		$\text{pF}$
Gate-Source Charge	$Q_{gs}$			4.2		
Gate-Drain Charge	$Q_{gd}$			4		
Input Capacitance	$C_{iss}$	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1013		$\text{pF}$
Output Capacitance	$C_{oss}$			134		
Reverse Transfer Capacitance	$C_{rss}$			88		
<b>Switching Characteristics<sup>(3)</sup></b>						
Turn-On Delay Time	$T_{d(on)}$	$V_{DS} = 15\text{V}, I_D = 1\text{A}, V_{GS} = 10\text{V}, R_G = 3.3\Omega$		13		$\text{nS}$
Rise Time	$T_r$			14		
Turn-Off Delay Time	$T_{d(off)}$			45		
Fall Time	$T_f$			9		
<b>Diode Characteristics</b>						
Maximum Continuous Drain-Source Diode Forward Current	$I_S$				50	A
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0\text{V}, I_S = 1\text{A}$		0.7	1	V

### Notes:

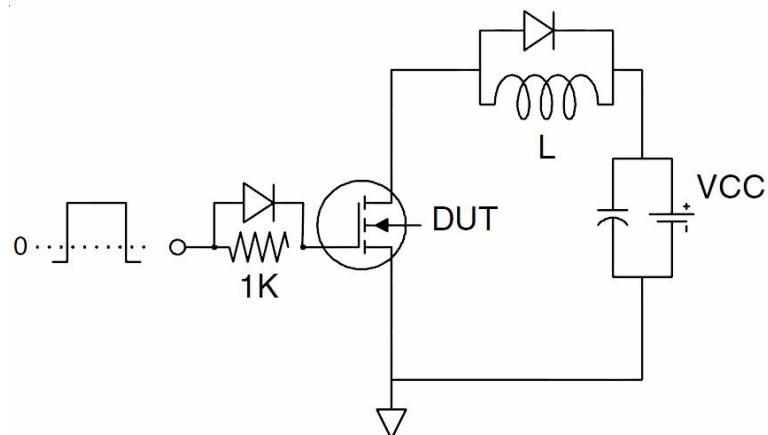
1. Pulse width < 300us, Duty cycle < 2%.
2. Essentially independent of operating temperature typical characteristics.
3. Repetitive rating, pulse width limited by junction temperature  $T_J(\text{MAX}) = 150^\circ\text{C}$ . Ratings are based on low frequency and duty cycles to keep initial  $T_J = 25^\circ\text{C}$ .
4. The maximum current rating is package limited.
5.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch<sup>2</sup> with 2oz.square pad of copper.
6. The test condition is  $L = 0.1\text{mH}, I_{AS} = 38\text{A}, V_{DD} = 25\text{V}, V_{GS} = 10\text{V}$ , Starting  $T_J = 250^\circ\text{C}$ .
7. Guaranteed by design, not subject to production testing.

## Test Circuits

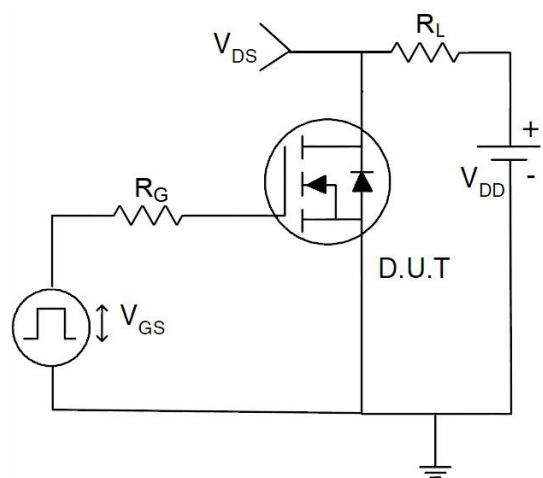
- EAS Test Circuits



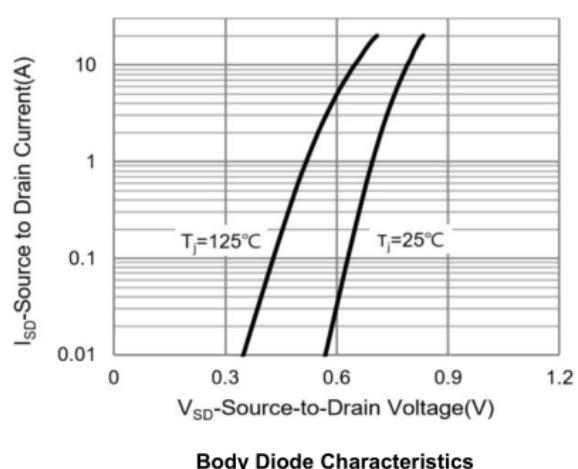
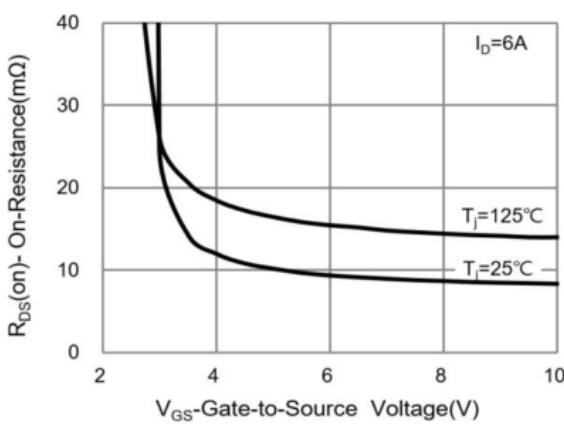
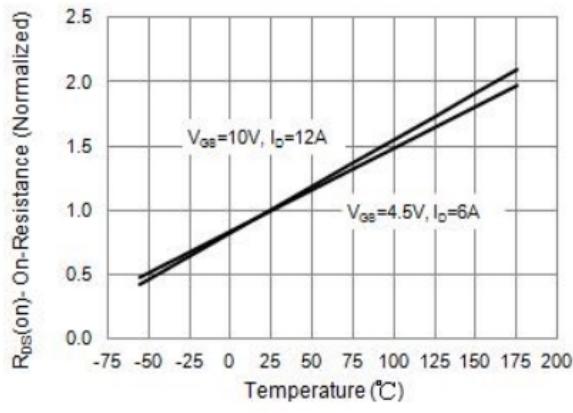
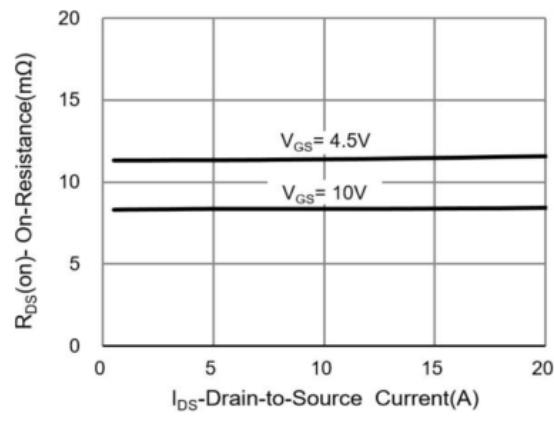
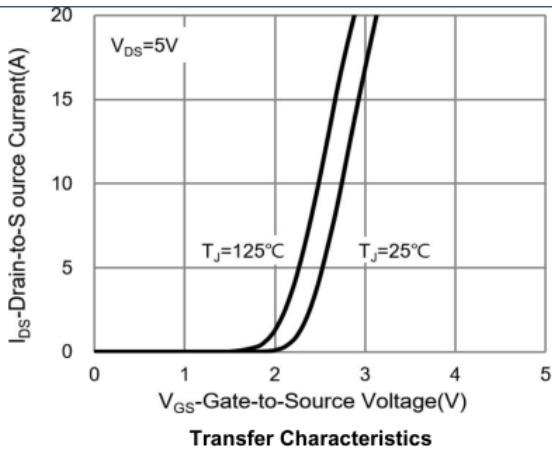
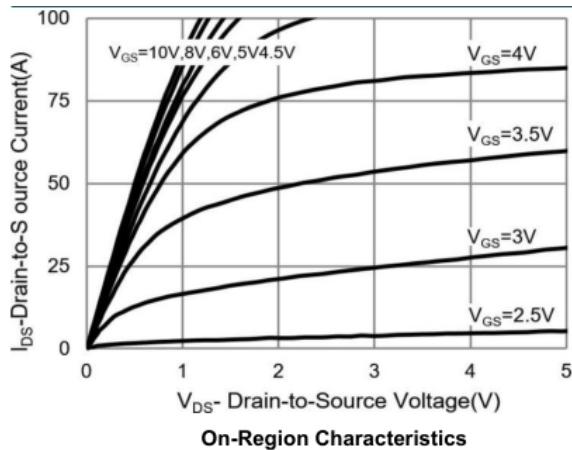
- Gate Charge Test Circuit

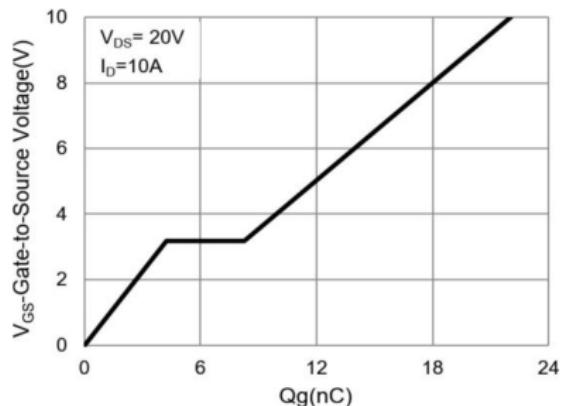


- Switch Time Test Circuit

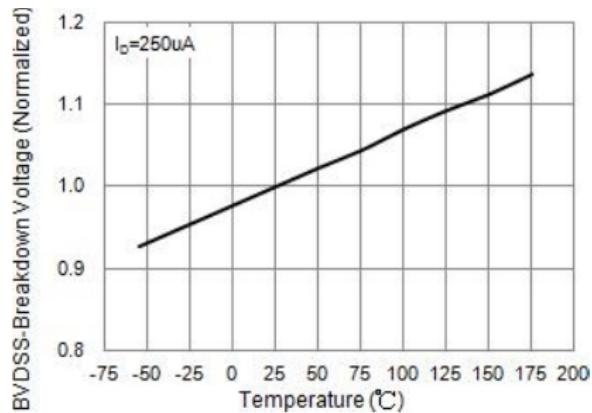


## Typical Characteristics

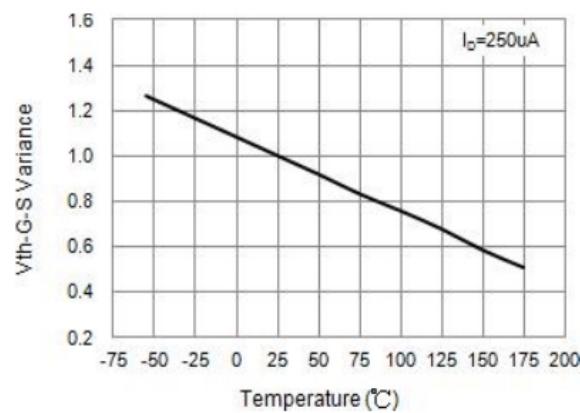




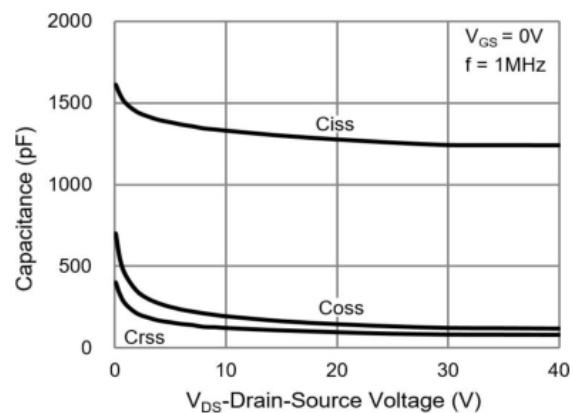
Gate-Charge Characteristics



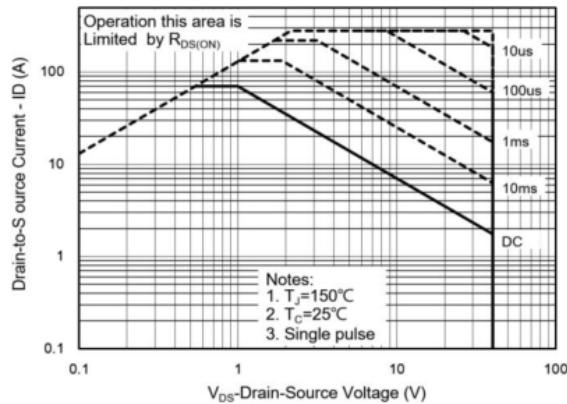
Breakdown Voltage Variation vs. Temperature



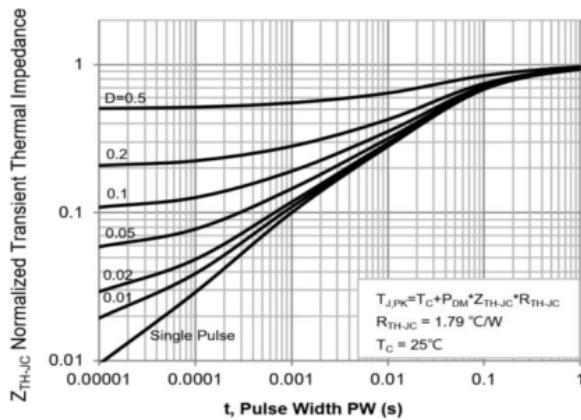
Threshold Voltage Variation with Temperature



Capacitance vs. Drain-Source Voltage

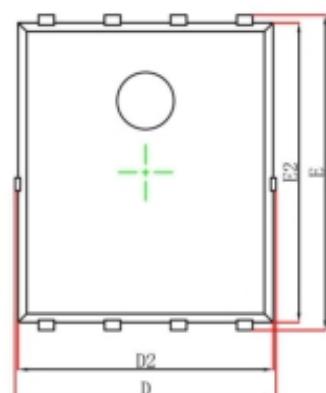


Maximum Safe Operating Area

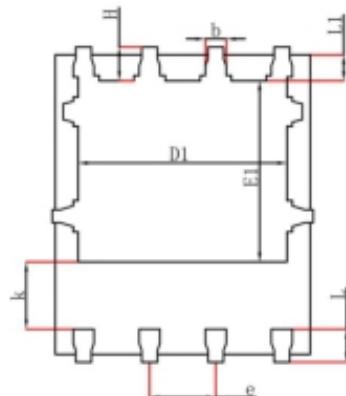


Normalized Transient Thermal Impedance

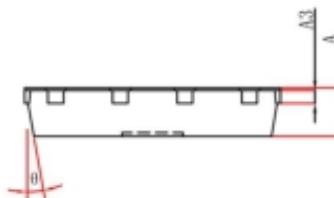
## PDFNWB5X6-8L Package Information



Top View  
[顶视图]



Bottom View  
[背视图]



Side View  
[侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
$\theta$	10°	12°	10°	12°